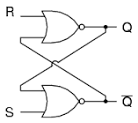
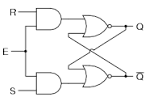
**EE 2420 Lab Guide 3: Latches**

**Example Overview:**

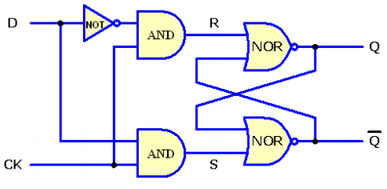
Design an SR latch, gated SR latch, and D flip-flop using Verilog HDL.

The purpose of latches is for memory. Depending on the input, the output will

“remember” the previous input. Think of it as a 1 bit memory chip.

* *

SR Latch Gated SR Latch

**

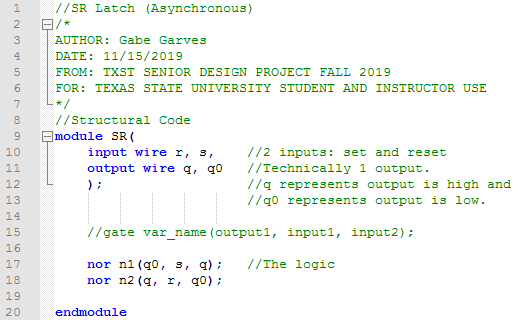
D Flip-Flop

**Figure 1**

**Verilog Code Breakdown:**

The SR latch only uses 2 NOR gates. The inputs of the NOR gate is the

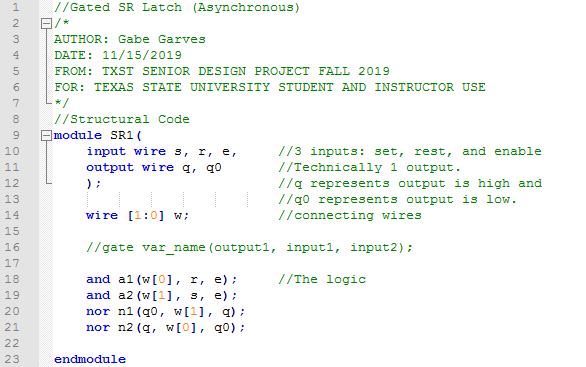
output of the other NOR gate and either S or R.



**Figure 2**

The Gated SR latch is very similar to the SR latch. The difference is two AND

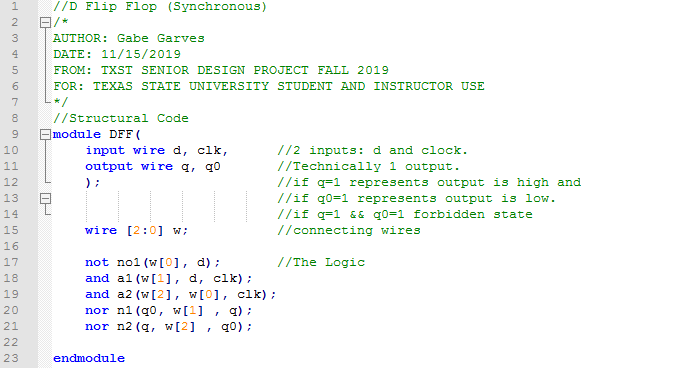
gates. The inputs of the NAND gates are E and either S or R. Output feeds into the SR latch.



**Figure 3**

The D flip-flop is very similar to the Gated SR latch with a few tweaks. Instead of an

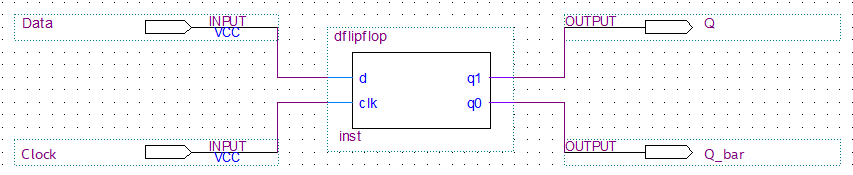
enable, you have a clock. S and R are replaced by D.



**Figure 4**

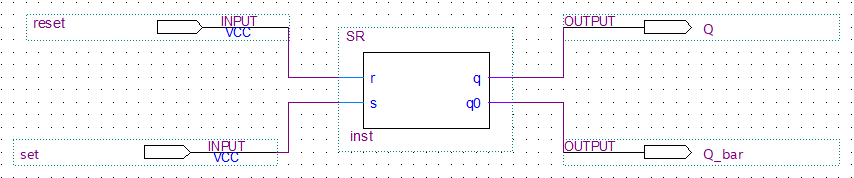
**FPGA Implementation:**

Using your knowledge from the previous two labs, implement your verilog code into a **symbol** for each latch. Use any of the orange pins in **Figure 8** as a guide when pin planning the latches. Use **Figures 5, 6** and **7** to get an idea of how the **inputs** and **outputs** to connect with the **symbols** in a **block diagram**. Your **outputs** will go the the on-board **LEDs.**

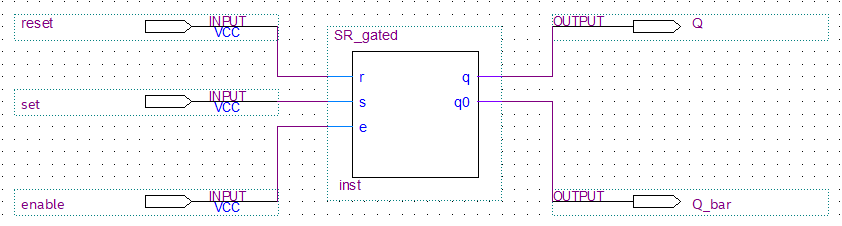


**Figure 5**

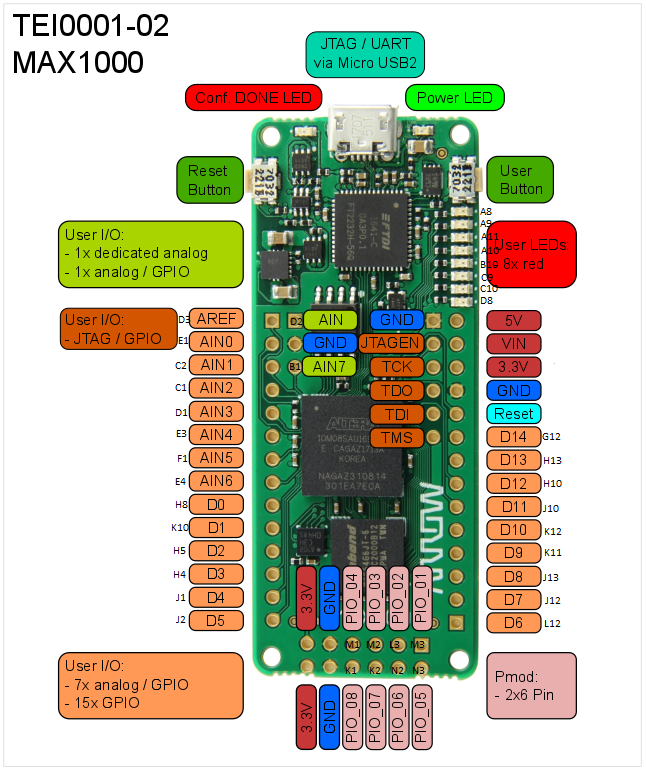
*It is recommended to create a single* ***.bdf*** *file where you can insert, compile, and program each latch separately onto the Max10. This will allow you to see each latch function individually and reduce the complexity of the project.*

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**Figure 6**

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**Figure 7**



**Figure 8**